WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first transistor;

a second transistor arranged electrically in parallel with said first transistor;

a first diode group including a plurality of diode elements connected electrically in parallel with each other to a first terminal of said first transistor; and

a second diode group including a plurality of diode elements electrically connected in parallel with each other to a first terminal of said second transistor, a center of gravity made by the diode elements in said second diode group overlapping in position with a center of gravity made by the diode elements in said first diode group.

2. The semiconductor device according to claim 1, wherein the first and second transistors each have a second terminal connected to a common node.

3. The semiconductor device according to claim 1, wherein the first and second transistors each receive, at the first terminal, a different internal signal via a different internal line.

4. The semiconductor device according to claim 1, wherein the first and second transistors each comprise an insulated gate field effect transistor and said first terminal is a control electrode node of said insulated gate field effect transistor.

5. The semiconductor device according to claim 1, wherein

the plurality of diode elements in said first diode group comprise a plurality of first impurity regions of a second conductivity type, arranged being spaced away from each other on a surface of a first semiconductor substrate region of a first conductivity type connected to a predetermined

voltage, being connected to the first terminal of said first transistor,

the plurality of diode elements in said second diode group comprise a plurality of second impurity regions of the second conductivity type formed being spaced away from each other on the surface of said first semiconductor substrate region and connected to the first terminal of said second transistor, and

a position of center of gravity of said plurality of second impurity regions overlaps with a position of center of gravity of said plurality of first impurity regions.

6. The semiconductor device according to claim 5, wherein the first and second impurity regions are formed on the surface of said first semiconductor substrate region in a matrix of rows and columns.

7. The semiconductor device according to claim 6, wherein the first and second impurity regions are alternately arranged in said matrix of rows and columns.

8. The semiconductor device according to claim 5, wherein the first and second impurity regions are arranged one dimensionally in alignment.

9. The semiconductor device according to claim 8, wherein the first impurity regions are arranged with the second impurity regions being interposed in between.

10. The semiconductor device according to claim 5, wherein the first and second impurity regions are arranged corresponding to apexes of a rectangle so that the first impurity regions are arranged opposite with each other at positions of apexes on a first diagonal line of said rectangle and the second impurity regions are arranged opposite with each other at positions of apexes on a second diagonal line of said rectangle.

11. The semiconductor device according to claim 5, further

comprising a third impurity region of the first conductivity type formed, in said first semiconductor substrate region, surrounding the first and second impurity regions.

12. The semiconductor device according to claim 11, wherein said third impurity region is arranged outside an entire of the first and second impurity regions.

13. The semiconductor device according to claim 11, wherein said third impurity region is formed surrounding each of the first and second impurity regions.

14. The semiconductor device according to claim 11, wherein said third impurity region is continuously formed.

15. The semiconductor device according to claim 11, wherein said third impurity region includes a plurality of divided regions formed separately from each other.

16. The semiconductor device according to claim 1, wherein a first substrate region for forming the diode elements of the first and second diode groups is different in conductivity type from a second substrate region for forming the first and second transistors, and said first substrate region is biased so as to set the diode elements in said first and second diode groups to a reverse biased state.

17. The semiconductor device according to claim 1, wherein

the diode elements in the first and second diode groups are formed commonly in a first substrate region of a first conductivity type,

said semiconductor device further comprises a second substrate region of a second conductivity type formed surrounding said first substrate region,

the first and second substrate regions are set to a reverse biased

state, and

said second substrate region is different in conductivity type from a substrate region where the first and second transistors are formed.

18. The semiconductor device according to claim 1, wherein

the first and second transistors each include a plurality of transistor elements, the transistor elements being arranged surrounding a region where the diodes of the first and second diode groups are formed, and

a center of gravity of the transistor elements forming said first transistor overlaps in position with a center of gravity of the transistor elements forming said second transistor.

19. The semiconductor device according to claim 18, wherein

the plurality of diode elements in said first diode group comprise a plurality of first impurity regions arranged separate from each other on a surface of a substrate region,

the plurality of diode elements in said second diode group comprise a plurality of second impurity regions arranged separate from each other on the surface of said substrate region, and

an interconnection line connecting the transistor elements forming said first transistor and the first impurity regions is identical in at least one of length and geometrical feature to an interconnection line connecting the transistor elements forming said second transistor and the second impurity regions.

20. The semiconductor device according to claim 18, wherein an interconnection line connecting the transistor elements and corresponding impurity regions comprises an interconnection line in a lowest interconnection layer among available interconnection lines.